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09/752,122	12/29/2000	Shyh-An Chi	JCLA6705	8732

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EXAMINER	
O'BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,122	CHI ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 7-14 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: RCE as received on 8/09/2004.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: In Fig.3, reference characters 312, 342, 344, 352, 354, 362, and 372, and in Fig.4, reference characters 412 and 442. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Response to Arguments

6. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

7. Claims 1 and 5 are objected to because of the following informalities:

   a. Claim 1 recites the limitation, "an next instruction" on its tenth line. Please correct the claim language to read, "a next instruction" in order to be grammatically correct. Also see Claim 5, line 13, for a similar correction.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 2 and 10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10. Claim 2 recites the limitation, "the control signal indicates whether the instruction executed in the current stage is a taken branch instruction" on its second and third lines. However, the Specification describes the control signal as being an execution result (see Specification, p.10 lines 6-7), and is further used for determining if the instruction should be fetched from an external memory (see Specification, p.10 lines 9-12). Although the Specification notes that the control signal "must reflect" if it is a taken branch instruction, it does not describe the control signal as "indicating" that the instruction is a taken branch instruction. Thus, the specification has not described how the control signal "indicates" that an instruction is a taken branch instruction in a way to enable one of ordinary skill in the art to make or use the claimed invention. Claim 10 recites the same limitation as claim 2, and thus is rejected for the same reasons as above.

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-5 and 7-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Claim 1 recites the limitation, "the fetch instruction many not be fetched" on lines 15-16. This limitation is indefinite because it does not define clearly whether the instruction is fetched if

it is not stored in the cache memory, nor does it define the situation that would allow the fetch instruction to be fetched. Please clarify the claim language to more clearly define the metes and bounds of the claim language. The Examiner suggest that the claim language be stated more definitively, such as "if the fetch instruction is not stored in the cache memory, the fetch instruction is not fetched from the external memory", so as to more clearly define the situation that occurs when there is a cache miss. Also see claim 5 line 18, claim 9 line 12, and claim 12 line 13 for similar recitations that require correction. Dependent claims 2-4, 7-8, 10-11 and 13-14, respectively, contain all the limitations of their parent claims, and thus are rejected for the same reasons as above.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-5 and 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishimi et al., U.S. Patent No. 5,708,803.

16. Regarding claim 1, Ishimi has taught a memory data access structure in a processor, comprising:

a. A cache memory (3 of Fig.3), to store and output data according to an address signal (see Col.5 lines 44-47),

b. A pipeline processor (see Figs.1-2), for executing a plurality of processor instructions, the pipeline processor including an execution unit to perform an execution operation on the instruction input from a previous stage (see Col.4 lines 34-59), and to output a result signal (see Col.13 lines 33-41) and a control signal (57 of Fig.10), wherein the control signal is output to the cache memory (see Col.12 lines 51-61). Here, there is inherently a "result signal" output from the execution unit that is used in determining if the branch prediction was correct.

c. Wherein when the instruction executed by the execution unit is a branch instruction, the result signal is a target address, wherein the target address is selected to be an address signal output to the cache memory, wherein the cache memory fetches a next data according to the address signal (see Col.11 line 44 – Col.12 line 28 and Col.13 lines 33-41),

d. When the execution unit is executing the branch instruction, the processor is fetching a data from the cache memory, and when the control signal obtained after executing the branch instruction is output to the cache memory, if the data is not stored in the cache memory, the data may not be fetched from the external memory to the cache memory according to the control signal (see Col.12 lines 51-61, Col.13 lines 27-41 and Col.14 lines 8-11).

17. Ishimi has not taught wherein the cache memory stores and outputs instructions according to control and result signals.

18. However, Ishimi has taught that the cache memory and the method to access it that is relied upon in the above rejection can also be extended to an instruction cache and a method of

fetching instructions from it. Because Ishimi has taught that the data cache and the method of accessing it can be applied to an instruction cache, one of ordinary skill in the art would have found it obvious to modify the data cache and method of accessing it to be an instruction cache and corresponding instruction fetching method.

19. Regarding claim 2, Ishimi has taught the memory data access structure according to claim 1 as shown above, wherein the control signal indicates whether the instruction executed in the current stage is a taken branch instruction (see Col.12 lines 51-61). Here, the fetch request signal indicates that the branch prediction has been assured and it sends a signal to the cache to request the data.

20. Regarding claim 3, Ishimi has taught the memory data access structure according to claim 1 as shown above, further comprising a program counter (see 23 of Fig.1) to store an address of the instruction currently executed among all the instructions to be executed (see Col.4 lines 21-26). Here, there is inherently a program counter in the system if there is a "program counter calculation unit". Ishimi has not explicitly taught, though, that the program counter stores an address of the currently executed instruction.

21. However, "Official Notice" is taken that it is well known and conventional in the art that a program counter keeps track of the instruction currently being executed. Therefore, because Ishimi has taught a program counter, one of ordinary skill in the art would have found it obvious to modify the program counter to keep track of the instruction currently being executed.

22. Regarding claim 4, Ishimi has taught the memory data access structure according to claim 3 as shown above, further comprising a multiplexer to receive the result signal output by the execution unit and the executed address stored in the program counter plus a set value, and to

select one of the signals as the address signal (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, although a multiplexer is not explicitly taught, there is inherently a "multiplexing" operation taking place when the branch prediction is validated, as if the branch is taken the result signal is used as the address, and if the branch is not taken the next sequential instruction (PC + a value) is used as the address.

23. Regarding claim 5, Ishimi has taught a memory data access structure in a processor, comprising:

a. A cache memory (3 of Fig.3), to store and output an instruction according to an address signal (see Col.5 lines 44-47),

b. A pipeline processor (see Figs.1-2), for executing a plurality of processor instructions, including an execution unit to perform an execution operation on an instruction transferred from a previous stage (see Col.4 lines 34-59), and to output a result signal (see Col.13 lines 33-41). Here, there is inherently a "result signal" output from the execution unit that is used in determining if the branch prediction was correct.

c. A branch instruction prediction mechanism, to output a predicted address according to a fetch instruction, which is an instruction to be fetched (see Col.4 lines 47-51),

d. A comparator, to receive the result signal and the predicted address and to output a comparison signal (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, although a comparator is not explicitly taught, there is inherently a "comparison" operation taking place when the branch prediction is validated, as if the branch is

taken the result signal is used as the address, and if the branch is not taken the next sequential instruction (PC + a value) is used as the address.

e. Wherein when the execution unit is executing a branch instruction, the result signal is a target address, wherein the target address is selected to be an address signal output to the cache memory, wherein an next instruction to be executed is fetched according to the address signal (see Col.11 line 44 – Col.12 line 28 and Col.13 lines 33-41),

f. When the execution unit is executing the branch instruction, the processor fetches the fetch instruction, and the result signal obtained after executing the branch instruction is transferred to the comparator, the comparator then outputs the comparison signal to the cache memory according to the result signal and the predicted address, if the fetch instruction is not stored in the cache memory, the fetch instruction may not be fetched from the external memory to the cache memory according to the comparison signal (see Col.12 lines 51-61, Col.13 lines 27-41 and Col.14 lines 8-11).

24. Regarding claim 7, Ishimi has taught the memory data access structure according to claim 5 as shown above, further comprising a program counter (see 23 of Fig.1) to store an address of an instruction which is executed currently among all the instruction to be executed (see Col.4 lines 21-26). Here, there is inherently a program counter in the system if there is a "program counter calculation unit". Ishimi has not explicitly taught, though, that the program counter stores an address of the currently executed instruction.

25. However, "Official Notice" is taken that it is well known and conventional in the art that a program counter keeps track of the instruction currently being executed. Therefore, because Ishimi has taught a program counter, one of ordinary skill in the art would have found it obvious to modify the program counter to keep track of the instruction currently being executed.

26. Regarding claim 8, Ishimi has taught the memory data access structure according to claim 7, comprising further a multiplexer to receive the result signal output from the execution unit, an execution address stored in the program counter plus a signal with a determined value, and the predicted address, and to select one of these signals as an address signal (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, although a multiplexer is not explicitly taught, there is inherently a "multiplexing" operation taking place when the branch prediction is validated, as if the branch is taken the result signal is used as the address, and if the branch is not taken the next sequential instruction (PC + a value) is used as the address.

27. Regarding claim 9, Ishimi has taught a method of memory data access in a processor, comprising:

a. Providing data according to an address signal (see Col.5 lines 44-47),

b. Executing the instruction (see Col.4 lines 34-59) to output a result signal (see Col.13 lines 33-41) and a control signal (19 of Fig.10). Here, there is inherently a "result signal" output from the execution unit that is used in determining if the branch prediction was correct (see Col.12 lines 51-61).

c. Fetching a next data according to an address signal, wherein when the instruction is a branch instruction, the result signal is a target address, wherein the target

address is selected to be the address signal output to a cache memory (see Col.11 line 44 – Col.12 line 28 and Col.13 lines 33-41),

d. Determining whether a data is fetched from an external memory according to the control signal when the processor is fetching the data and the data is not stored in the cache memory,

e. Wherein when the data is not stored in the cache memory, the data may not be fetched form the external memory because the control signal prevents the cache memory from doing so (see Col.12 lines 51-61, Col.13 lines 27-41 and Col.14 lines 8-11).

28. Ishimi has not taught wherein the cache memory stores and outputs instructions according to control and result signals.

29. However, Ishimi has taught that the cache memory and the method to access it that is relied upon in the above rejection can also be extended to an instruction cache and a method of fetching instructions from it. Because Ishimi has taught that the data cache and the method of accessing it can be applied to an instruction cache, one of ordinary skill in the art would have found it obvious to modify the data cache and method of accessing it to be an instruction cache and corresponding instruction fetching method.

30. Regarding claim 10, Ishimi has taught the method according to claim 9 as shown above, wherein the control indicates whether the instruction currently executed is a taken branch instruction (see Col.12 lines 51-61). Here, the fetch request signal indicates that the branch prediction has been assured and it sends a signal to the cache to request the data.

31. Regarding claim 11, Ishimi has taught the method according to claim 9 as shown above, comprising further the step of selectively outputting the result signal and an address of the instruction executed currently plus a signal with a certain value (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, there is inherently a "multiplexing" operation taking place when the branch prediction is validated, as if the branch is taken the result signal is selected to be the address, and if the branch is not taken the next sequential instruction (PC + a value) is selected to be the address.

32. Regarding claim 12, Ishimi has taught a method for memory data access in a processor, comprising:

a. Providing an instruction (see Col.5 lines 44-47),

b. Executing the instruction to output a result signal (see Col.4 lines 34-59 and Col.13 lines 33-41). Here, there is inherently a "result signal" output from the execution unit that is used in determining if the branch prediction was correct.

c. Using a branch prediction mechanism to receive a fetch instruction, which is an instruction to be fetched, and to output a predicted address (see Col.4 lines 47-51),

d. Comparing the result signal with the predicted address, and outputting a comparison signal (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, there is inherently a "comparison" operation taking place when the branch prediction is validated, as if the branch is taken the result signal is used as the address, and if the branch is not taken the next sequential instruction (PC + a value) is used as the address.

e. Wherein when the instruction being executed is a branch instruction, the result signal is a target address and is selected to be an address signal, the processor fetches an instruction to be executed next according to the address signal (see Col.11 line 44 – Col.12 line 28 and Col.13 lines 33-41),

f. While executing the branch instruction, the processor fetches the fetch instruction, if the fetch instruction is not in a cache memory, according to the comparison signal, the cache memory may not fetch the fetch instruction from an external memory (see Col.12 lines 51-61, Col.13 lines 27-41 and Col.14 lines 8-11).

33. Regarding claim 13, Ishimi has taught the method according to claim 12 as shown above, comprising further a step of selectively outputting one of the result signals, an address that the processor is currently processing plus a certain value, and the predicted address (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, there is inherently a "multiplexing" operation taking place when the branch prediction is validated, as if the branch is taken the result signal is selected to be the address, and if the branch is not taken the next sequential instruction (PC + a value) is selected to be the address.

34. Regarding claim 14, Ishimi has taught the method according to claim 12 as shown above, wherein the comparison signal indicates whether the branch instruction predicted by the branch prediction mechanism is correct (see Col.12 lines 51-61 and Col.13 lines 33-41). Here, because a validation of the branch prediction is occurring, the output of the validation is inherently a signal that indicates whether the prediction was correct, so that appropriate action can take place, i.e. execute either the branch path or fall-through path.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. After October 12th, 2004, the examiner can be reached at (571) 272-4171. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm, with the exception of first Friday of every bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached at (703) 305-9712, or at (571) 272-4162 on or after October 12th, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien

Examiner
Art Unit 2183

BJO
10/7/2004

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